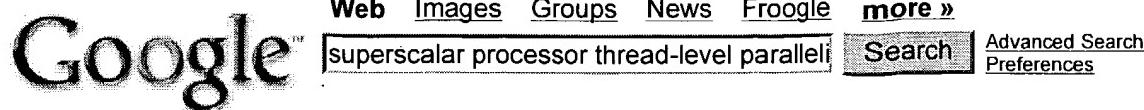


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3	2	multi\$thread\$1 near processor\$1 same part\$1	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:17
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7	6	multi\$thread\$1 near processor\$1 same execut\$4 same decode\$2	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:36
8	183	(multi\$thread\$1 or super\$scalar) near processor\$1 same execut\$4 same decode\$2	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:36
9	180	super\$scalar near processor\$1 same execut\$4 same decode\$2	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:37
10	50	712/22,23,24.ccls. and (super\$scalar near processor\$1 same execut\$4 same decode\$2)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:36
11	46	(712/22,23,24.ccls. and (super\$scalar near processor\$1 same execut\$4 same decode\$2)) and @ay <= "2001"	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:37
12	52	super\$scalar near processor\$1 same decode\$2 same execut\$4 near units	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:38
13	20	712/22,23,24.ccls. and (super\$scalar near processor\$1 same decode\$2 same execut\$4 near units)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/17 10:38
-	2	(ILP sane SMP same alternatively) and (storage with (buffer\$1 or locations) same thread\$1 same data)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/15 12:51
-	1	(ILP sane SMP same super\$scalar near2 processor\$1) and (storage with (buffer\$1 or locations) same thread\$1)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/15 12:52

	71	(ILP sane SMP same super\$scalar near2 processor\$1) and (storage with (buffer\$1 or locations) same data)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/15 13:32
	3	(712/22,23,24.ccls. or 718/1,104,,105,106,107.ccls.) and ((ILP sane SMP same super\$scalar near2 processor\$1) and (storage with (buffer\$1 or locations) same data))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/15 13:32



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### "Converting Thread-Level Parallelism to Instruction-Level ..."

... multiple-issue hardware on a **superscalar** is wasted. ... parallel applications on an SMT **processor** is its ability to use **thread-level parallelism** and instruction ...

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... Converting **Thread-Level Parallelism** Into Instruction-Level **Parallelism** via ... or 2 to 4 **superscalar** processors on ... chip) are another emerging **processor** design that ...

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... form of **parallelism** is called **Thread Level Parallelism** or TLP. ... or programs on a single **processor** by running ... in a four way **superscalar processor** (unused slots ...

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... Alpha EV8 (Part 3): **Simultaneous** Multi-Threat. ... to MPU design that can exploit **thread level parallelism** (TLP ... 3 or 4 issue wide **superscalar processor** core shipping ...

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### [PDF] Exploiting Speculative Thread-Level Parallelism on a SMT processor

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... higher performance than a **superscalar processor** using the ... fact that all **simultaneous** threads are ... architecture to exploit **thread-level parallelism**, in addition ...

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### Converting Thread-Level Parallelism to Instruction-Level ...

... Tullsen", title = "Converting **Thread-Level Parallelism** to Instruction ... 1993 127

**superscalar** microprocessor (context ... 66 An elementary **processor** architecture with ...

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... 13. **Simultaneous** Multithreading (SMT). ... ie, convert **thread-level parallelism** into more ILP. ... 6.44 HP3). A **superscalar processor** with no multithreading. ...

[www.cs.unc.edu/~montek/teaching/fall-03/lectures/lecture-25.ppt](http://www.cs.unc.edu/~montek/teaching/fall-03/lectures/lecture-25.ppt) - Similar pages

### [PPT] Simultaneous Multithreading

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... Choice: Instruction Fetch and Issue on an Implementable **Simultaneous** Multithreading **Processor** , in Proceedings of ... **Thread Level Parallelism** (TLP). ... **Superscalar** ...

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### Converting Thread-Level Parallelism to Instruction-Level ...

... is a way to exploit both **thread level parallelism** <TLP> and ... units were swamped on another **processor** within the ... of building a wide issue **superscalar** SMT really ...

[www.cs.wisc.edu/~david/courses/cs838/notes/09-18-03.html](http://www.cs.wisc.edu/~david/courses/cs838/notes/09-18-03.html) - 19k - Cached - Similar pages

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... applying only a reasonable number of changes to a modern **superscalar processor** ...

Exploiting Speculative **Thread-Level Parallelism** on a SMT processor by Pedro ...

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